

LP3990 150mA Linear Voltage Regulator for Digital Applications

Check for Samples: [LP3990](#)

FEATURES

- 1% Voltage Accuracy at Room Temperature
- Stable with Ceramic Capacitor
- Logic Controlled Enable
- No Noise Bypass Capacitor Required
- Thermal-Overload and Short-Circuit Protection

KEY SPECIFICATIONS

- Input Voltage Range, 2.0 to 6.0V
- Output Voltage Range, 0.8 to 3.3V
- Output Current, 150mA
- Output Stable - Capacitors, 1.0 μ F
- Virtually Zero I_Q (Disabled), <10nA
- Very Low I_Q (Enabled), 43 μ A
- Low Output Noise, 150 μ V_{RMS}
- PSRR, 55dB at 1kHz
- Fast Start Up, 105 μ s

PACKAGE

All available in Lead Free option.

- 4-Pin DSBGA, 1 mm x 1.3 mm
- 6-pin WQFN (SOT-23 Footprint)
- SOT-23

For other package options contact your Texas Instruments sales office.

APPLICATIONS

- Cellular Handsets
- Hand-Held Information Appliances

DESCRIPTION

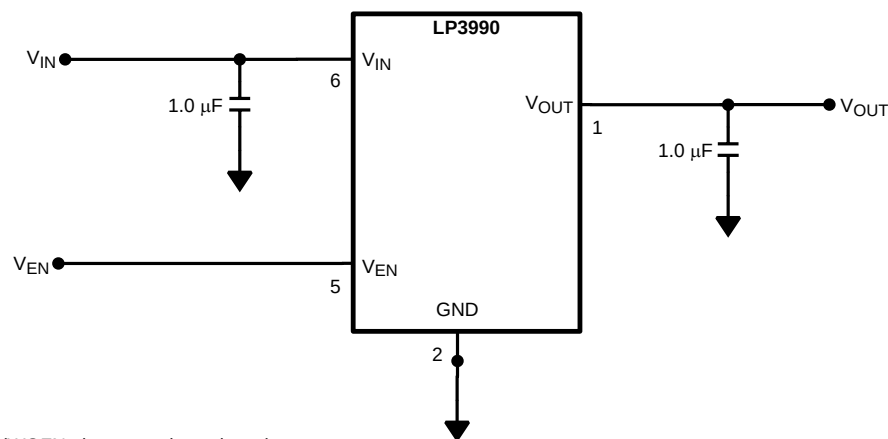
The LP3990 regulator is designed to meet the requirements of portable, battery-powered systems providing an accurate output voltage, low noise, and low quiescent current. The LP3990 will provide a 0.8V output from the low input voltage of 2V at up to 150mA load current. When switched into shutdown mode via a logic signal at the enable pin, the power consumption is reduced to virtually zero.

The LP3990 is designed to be stable with space saving ceramic capacitors as small as 1.0 μ F.

Performance is specified for a -40°C to 125°C junction temperature range.

For output voltages other than 0.8V, 1.2, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, or 3.3V please contact your local NSC sales office.

Typical Application Circuit



(WQFN pin connections shown)

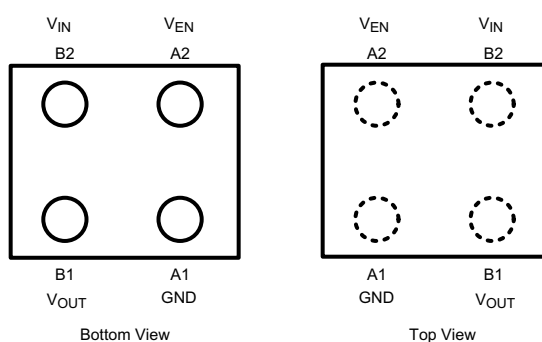


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

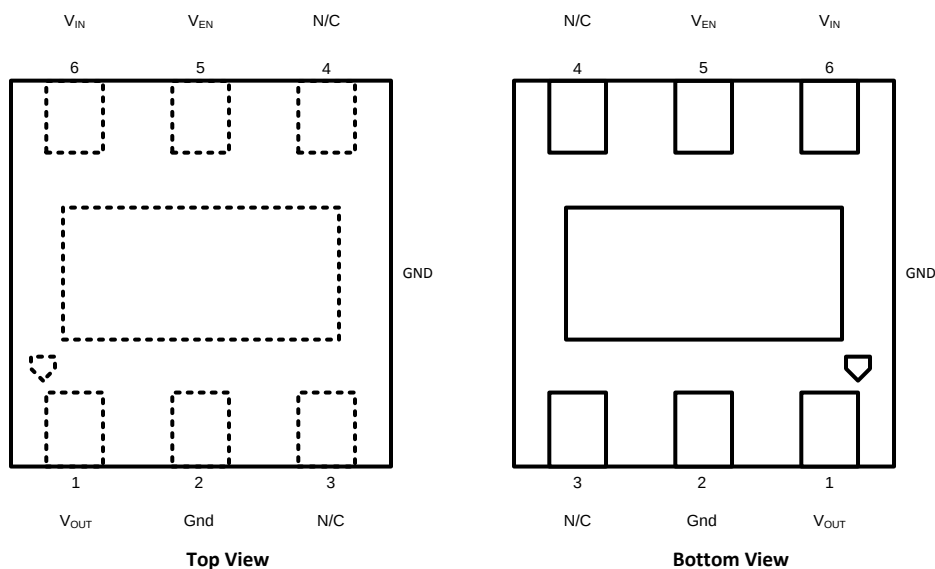
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PIN DESCRIPTIONS

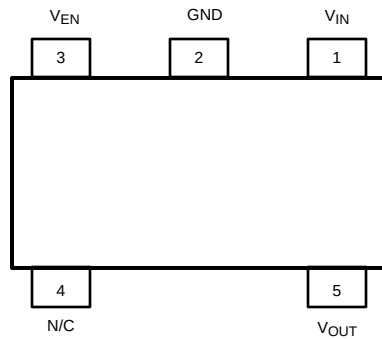
Pin No			Symbol	Name and Function
WQFN	DSBGA	SOT-23		
5	A2	3	V_{EN}	Enable Input; Enables the Regulator when $\geq 0.95V$. Disables the Regulator when $\leq 0.4V$. Enable Input has $1M\Omega$ pulldown resistor to GND.
2	A1	2	GND	Common Ground. Connect to Pad.
1	B1	5	V_{OUT}	Voltage output. A $1.0\mu F$ Low ESR Capacitor should be connected to this Pin. Connect this output to the load circuit.
6	B2	1	V_{IN}	Voltage Supply Input. A $1.0\mu F$ capacitor should be connected at this input.
3		4	N/C	No Connection. Do not connect to any other pin.
4			N/C	No Connection. Do not connect to any other pin.
Pad			GND	Common Ground. Connect to Pin 2.

Connection Diagram

DSBGA, 4 Bump Package
See Package Number YZR0004



WQFN-6 Package
See Package Number NGG0006A



SOT-23 Package
See Package Number DBV



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

Input Voltage	-0.3 to 6.5V
Output Voltage	-0.3 to ($V_{IN} + 0.3V$) with 6.5V (max)
Enable Input Voltage	-0.3 to ($V_{IN} + 0.3V$) with 6.5V (max)
Junction Temperature	150°C
Lead/Pad Temp. ⁽⁴⁾	
WQFN/SOT-23	235°C
DSBGA	260°C
Storage Temperature	-65 to 150°C
Continuous Power Dissipation Internally Limited ⁽⁵⁾	
ESD ⁽⁶⁾	
Human Body Model	2KV
Machine Model	200V

- (1) All Voltages are with respect to the potential at the GND pin.
- (2) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
- (3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (4) For further information on these packages please refer to the following Application Notes; AN1112 DSBGA Package Wafer Level Chip Scale Package, AN1187 Leadless Leadframe Package.
- (5) Internal thermal shutdown circuitry protects the device from permanent damage.
- (6) The human body model is 100pF discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Operating Ratings⁽¹⁾

Input Voltage	2V to 6V
Enable Input Voltage	0 to ($V_{IN} + 0.3V$) with 6.0V (max)
Junction Temperature	-40°C to 125°C
Ambient Temperature T_A Range ⁽²⁾	-40°C to 85°C

- (1) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) The maximum ambient temperature ($T_{A(max)}$) is dependant on the maximum operating junction temperature ($T_{J(max-op)} = 125°C$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max-op)} - (\theta_{JA} \times P_{D(max)})$.

Thermal Properties⁽¹⁾

Junction To Ambient Thermal Resistance ⁽²⁾	
$\theta_{JA}(\text{WQFN-6})$	88°C/W
$\theta_{JA}(\text{DSBGA})$	220°C/W
$\theta_{JA}(\text{SOT-23})$	220°C/W

- (1) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) Junction to ambient thermal resistance is dependant on the application and board layout. In applications where high maximum power dissipation is possible, special care must be paid to thermal dissipation issues in board design.

Electrical Characteristics

Unless otherwise noted, $V_{EN} = 950\text{mV}$, $V_{IN} = V_{OUT} + 1.0\text{V}$, or 2.0V , whichever is higher. $C_{IN} = 1\text{ }\mu\text{F}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 0.47\text{ }\mu\text{F}$.

Typical values and limits appearing in normal type apply for $T_J = 27^\circ\text{C}$. Limits appearing in **boldface** type apply over the full junction temperature range for operation, -40 to $+125^\circ\text{C}$. ⁽¹⁾

Symbol	Parameter	Conditions		Typ	Limit		Units
					Min	Max	
V _{IN}	Input Voltage	(2)			2	6	V
ΔV _{OUT}	Output Voltage Tolerance	I _{LOAD} = 1 mA	DSBGA		-1	+1	%
			WQFN		-1.5	+1.5	
			SOT-23		-1.5	+1.5	
		Over full line and load regulation.	DSBGA		-2.5	+2.5	
			WQFN		-3	+3	
			SOT-23		-4	+4	
	Line Regulation Error	V _{IN} = (V _{OUT(NOM)} + 1.0V) to 6.0V,		0.02	-0.1	0.1	%/V
	Load Regulation Error	I _{OUT} = 1mA to 150mA	V _{OUT} = 0.8 to 1.95V DSBGA	0.002	-0.005	0.005	%/mA
V _{OUT} = 0.8 to 1.95V WQFN, SOT-23			0.003	-0.008	0.008		
V _{OUT} = 2.0 to 3.3V DSBGA			0.0005	-0.002	0.002		
V _{OUT} = 2.0 to 3.3V WQFN, SOT-23			0.002	-0.005	0.005		
V _{DO}	Dropout Voltage	I _{OUT} = 150mA ⁽³⁾ ⁽⁴⁾		120		200	mV
I _{LOAD}	Load Current	See ⁽⁵⁾ ⁽⁴⁾			0		μA
I _Q	Quiescent Current	V _{EN} = 950mV, I _{OUT} = 0mA		43		80	μA
		V _{EN} = 950mV, I _{OUT} = 150mA		65		120	
		V _{EN} = 0.4V		0.002		0.2	
I _{SC}	Short Circuit Current Limit	See ⁽⁶⁾		550		1000	mA
I _{OUT}	Maximum Output Current				150		mA
PSRR	Power Supply Rejection Ratio	f = 1kHz, I _{OUT} = 1mA to 150mA		55			dB
		f = 10kHz, I _{OUT} = 150mA		35			
e _n	Output noise Voltage ⁽⁴⁾	BW = 10Hz to 100kHz,	V _{OUT} = 0.8	60			μV _{RMS}
			V _{OUT} = 1.5	125			
			V _{OUT} = 3.3	180			
T _{SHUTDOWN}	Thermal Shutdown	Temperature		155			°C
		Hysteresis		15			
Enable Control Characteristics							
I _{EN} ⁽⁷⁾	Maximum Input Current at V _{EN} Input	V _{EN} = 0.0V		0.001		0.1	μA
		V _{EN} = 6V		6	2.5	10	
V _{IL}	Low Input Threshold	V _{IN} = 2V to 6V				0.4	V
V _{IH}	High Input Threshold	V _{IN} = 2V to 6V			0.95		V

- (1) All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production at $T_J = 25^\circ\text{C}$ or correlated using Statistical Quality Control methods. Operation over the temperature specification is guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
- (2) $V_{IN(MIN)} = V_{OUT(NOM)} + 0.5\text{V}$, or 2.0V , whichever is higher.
- (3) Dropout voltage is voltage difference between input and output at which the output voltage drops to 100mV below its nominal value. This parameter only for output voltages above 2.0V .
- (4) This electrical specification is guaranteed by design.
- (5) The device maintains the regulated output voltage without the load.
- (6) Short circuit current is measured with V_{OUT} pulled to 0V and V_{IN} worst case = 6.0V .
- (7) Enable Pin has $1\text{M}\Omega$ typical, resistor connected to GND.

Electrical Characteristics (continued)

Unless otherwise noted, $V_{EN} = 950\text{mV}$, $V_{IN} = V_{OUT} + 1.0\text{V}$, or 2.0V , whichever is higher. $C_{IN} = 1\text{ }\mu\text{F}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 0.47\text{ }\mu\text{F}$.

Typical values and limits appearing in normal type apply for $T_J = 27^\circ\text{C}$. Limits appearing in **boldface** type apply over the full junction temperature range for operation, -40 to $+125^\circ\text{C}$. ⁽¹⁾

Symbol	Parameter	Conditions		Typ	Limit		Units
					Min	Max	
Timing Characteristics							
T _{ON}	Turn On Time ⁽⁸⁾	To 95% Level V _{IN(MIN)} to 6.0V	V _{OUT} = 0.8	80		150	μs
			V _{OUT} = 1.5	105		200	
			V _{OUT} = 3.3	175		250	
Transient Response	Line Transient Response δV _{OUT}	T _{rise} = T _{fall} = 30μs ⁽⁸⁾ δV _{IN} = 600mV		8		16	mV (pk - pk)
	Load Transient Response δV _{OUT}	T _{rise} = T _{fall} = 1μs ⁽⁸⁾ I _{OUT} = 1mA to 150mA C _{OUT} = 1μF		55		100	mV

(8) This electrical specification is guaranteed by design.

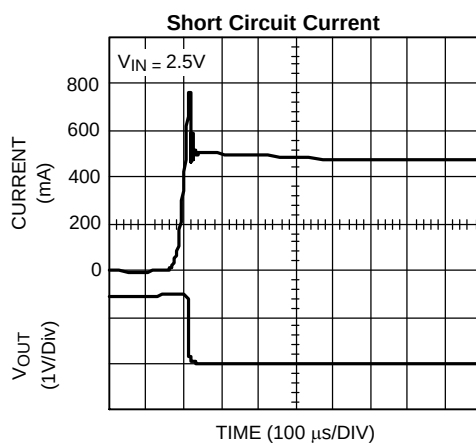
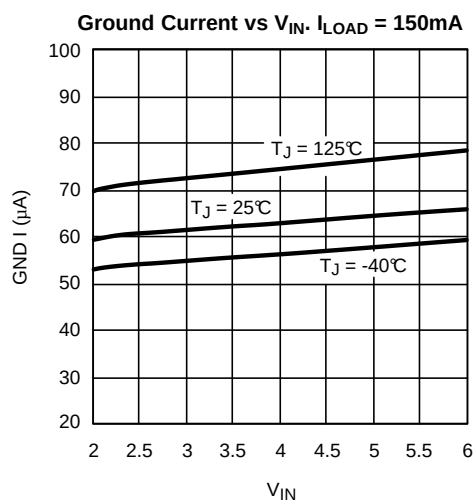
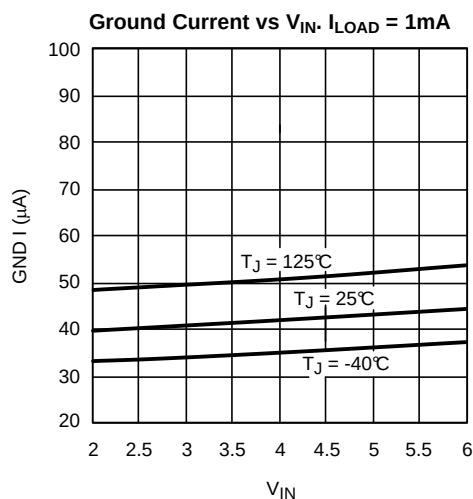
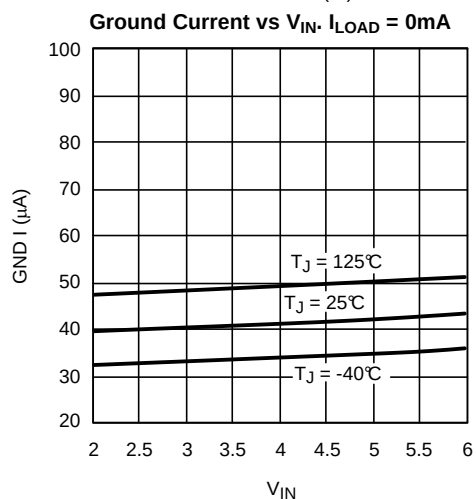
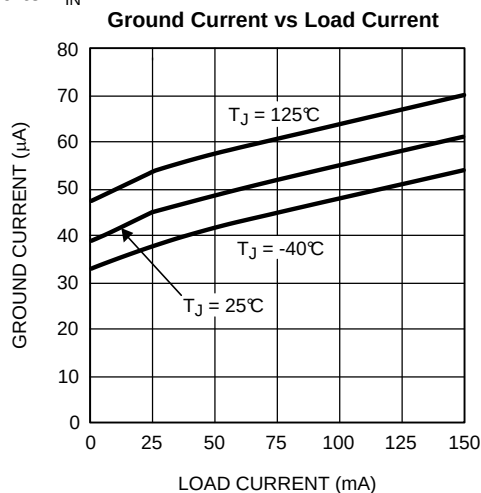
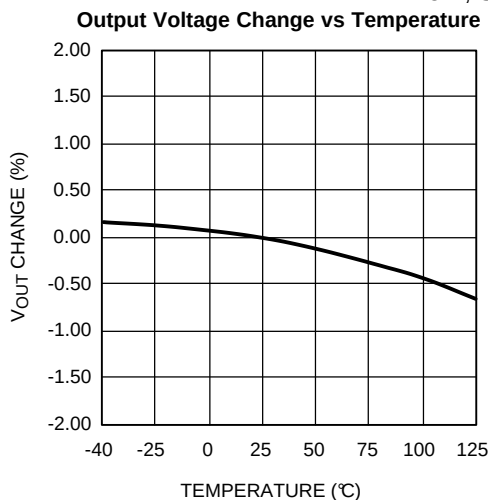
Output Capacitor, Recommended Specifications

Symbol	Parameter	Conditions	Nom	Limit		Units
				Min	Max	
C_{OUT}	Output Capacitance	Capacitance ⁽¹⁾	1.0	0.7		μF
		ESR		5	500	m Ω

(1) The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R. However, dependent on application, X5R, Y5V, and Z5U can also be used. (See [Application Hints](#))

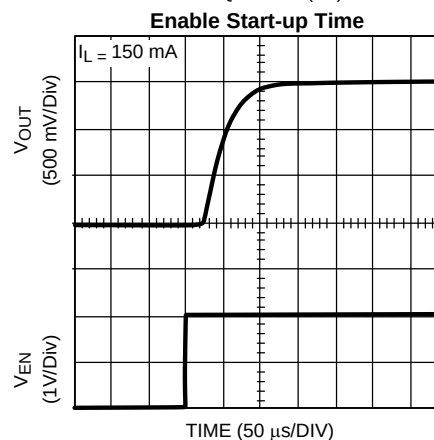
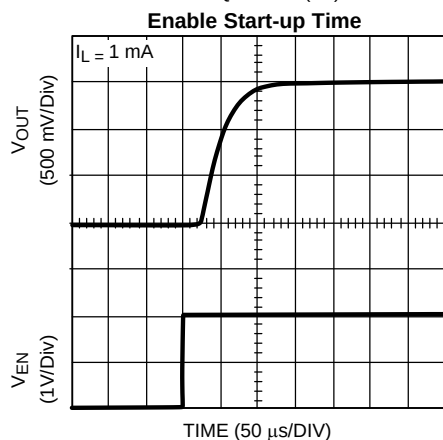
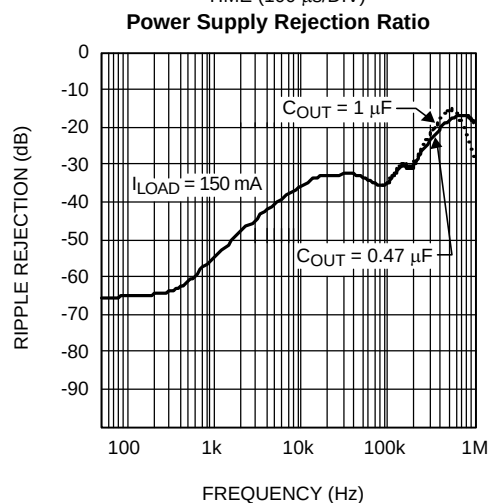
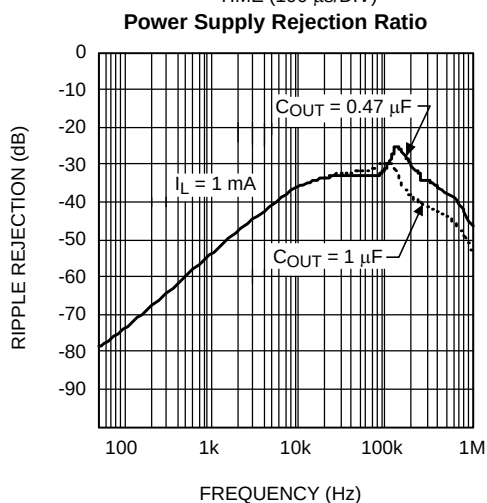
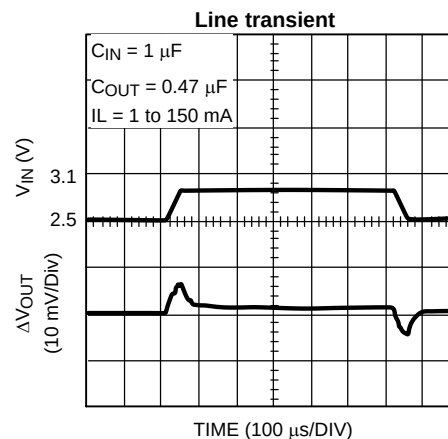
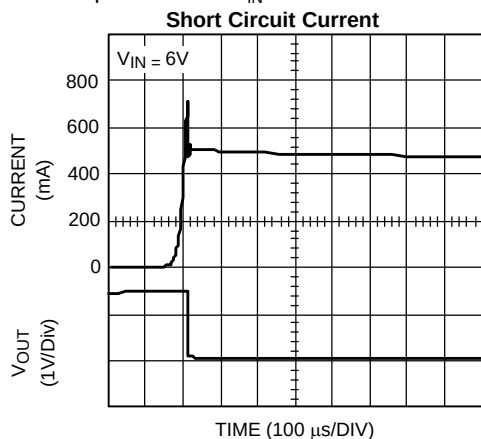
Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = 1.0\mu F$ Ceramic, $C_{OUT} = 0.47\mu F$ Ceramic, $V_{IN} = V_{OUT(NOM)} + 1.0V$, $T_A = 25^\circ C$, $V_{OUT(NOM)} = 1.5V$, Shutdown pin is tied to V_{IN} .



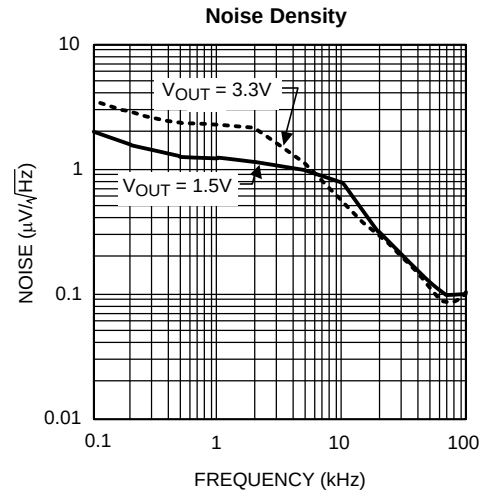
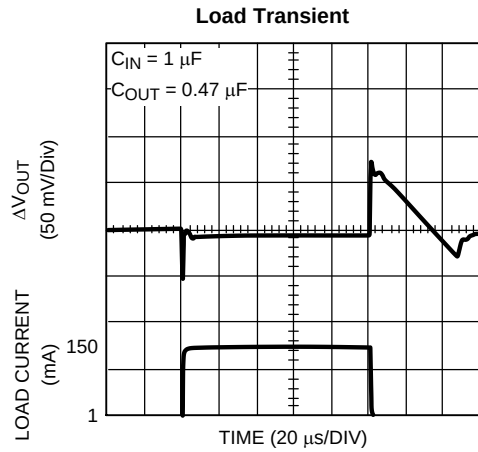
Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = 1.0\mu\text{F}$ Ceramic, $C_{OUT} = 0.47\mu\text{F}$ Ceramic, $V_{IN} = V_{OUT(NOM)} + 1.0\text{V}$, $T_A = 25^\circ\text{C}$, $V_{OUT(NOM)} = 1.5\text{V}$, Shutdown pin is tied to V_{IN} .



Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = 1.0\mu\text{F}$ Ceramic, $C_{OUT} = 0.47\mu\text{F}$ Ceramic, $V_{IN} = V_{OUT(NOM)} + 1.0\text{V}$, $T_A = 25^\circ\text{C}$, $V_{OUT(NOM)} = 1.5\text{V}$, Shutdown pin is tied to V_{IN} .



APPLICATION HINTS

EXTERNAL CAPACITORS

In common with most regulators, the LP3990 requires external capacitors for regulator stability. The LP3990 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0 μ F capacitor be connected between the LP3990 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB design practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are used to connect the battery or other power source to the LP3990, then it is recommended that the input capacitor is increased. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1.0 μ F over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3990 is designed specifically to work with very small ceramic output capacitors. A 1.0 μ F ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5m Ω to 500m Ω , is suitable in the LP3990 application circuit.

For this device the output capacitor should be connected between the V_{OUT} pin and ground.

It is also possible to use tantalum or film capacitors at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost (see [CAPACITOR CHARACTERISTICS](#)).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5m Ω to 500m Ω for stability.

NO-LOAD STABILITY

The LP3990 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP3990 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 μ F to 4.7 μ F, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1.0 μ F ceramic capacitor is in the range of 20m Ω to 40m Ω , which easily meets the ESR requirement for stability for the LP3990.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, [Figure 1](#) shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result

in the capacitance value falling below the minimum value given in the recommended capacitor specifications table (0.7 μ F in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

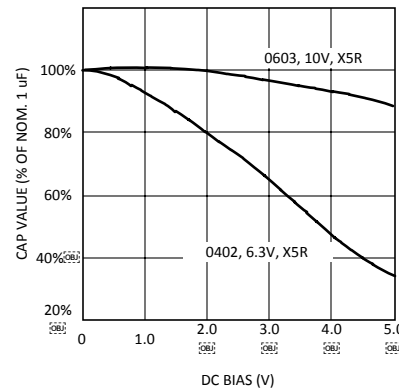


Figure 1. Graph Showing a Typical Variation in Capacitance vs DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to +125°C, will only vary the capacitance to within $\pm 15\%$. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55°C to +85°C. Many large value ceramic capacitors, larger than 1 μ F are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 μ F to 4.7 μ F range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

ENABLE CONTROL

The LP3990 features an active high Enable pin, V_{EN} , which turns the device on when pulled high. When not enabled the regulator output is off and the device typically consumes 2nA.

If the application does not require the Enable switching feature, the V_{EN} pin should be tied to V_{IN} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the [Electrical Characteristics](#) section under V_{IL} and V_{IH} .

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques, which are detailed in Application Note AN1112.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

DSBGA LIGHT SENSITIVITY

Exposing the DSBGA device to direct light may affect the operation of the device. Light sources, such as halogen lamps, can affect electrical performance, if placed in close proximity to the device.

Light with wavelengths in the infra-red portion of the spectrum is the most detrimental, and so, fluorescent lighting used inside most buildings, has little or no effect on performance.

REVISION HISTORY

Changes from Revision H (May 2013) to Revision I	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3990MF-1.2	ACTIVE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125	SCDB	Samples
LP3990MF-1.2/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCDB	Samples
LP3990MF-1.8	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	SCFB	Samples
LP3990MF-1.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCFB	Samples
LP3990MF-2.5	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	SCJB	Samples
LP3990MF-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCJB	Samples
LP3990MF-2.8	ACTIVE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125	SCKB	Samples
LP3990MF-2.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCKB	Samples
LP3990MF-3.3	ACTIVE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125	SCLB	Samples
LP3990MF-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCLB	Samples
LP3990MFX-1.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCDB	Samples
LP3990MFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCFB	Samples
LP3990MFX-3.3	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	SCLB	Samples
LP3990MFX-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCLB	Samples
LP3990SD-1.2	ACTIVE	WSO	NGG	6		TBD	Call TI	Call TI	-40 to 125	L086B	Samples
LP3990SD-1.2/NOPB	ACTIVE	WSO	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L086B	Samples
LP3990SD-1.5	ACTIVE	WSO	NGG	6		TBD	Call TI	Call TI	-40 to 125	L087B	Samples
LP3990SD-1.5/NOPB	ACTIVE	WSO	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L087B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3990SD-1.8	ACTIVE	WSO	NGG	6		TBD	Call TI	Call TI	-40 to 125	L088B	Samples
LP3990SD-1.8/NOPB	ACTIVE	WSO	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L088B	Samples
LP3990TL-0.8/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TL-1.2/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TL-1.35/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TL-1.5/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TL-1.8/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TL-2.5/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TL-2.8/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TLX-0.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TLX-1.2/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TLX-1.35/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TLX-1.5/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TLX-1.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TLX-2.5/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TLX-2.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

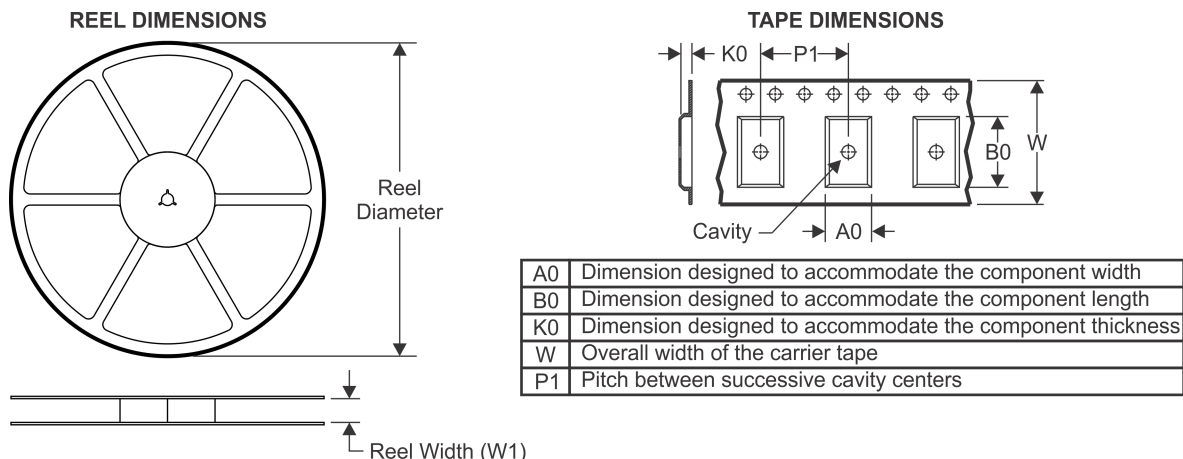
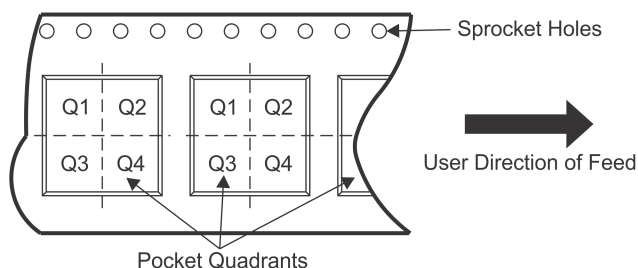
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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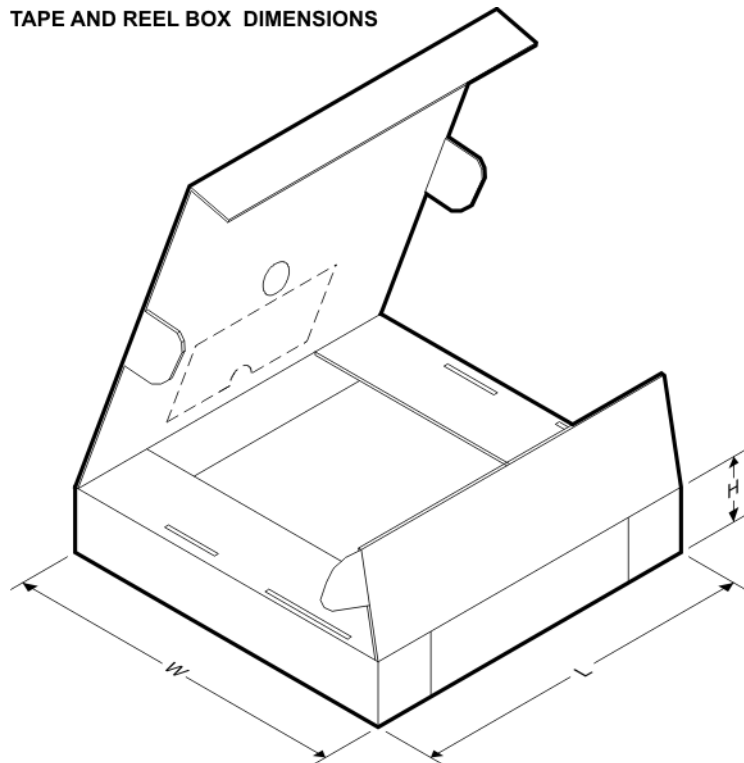
TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3990MF-1.2/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-1.8	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-1.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-2.5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-2.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MFX-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MFX-3.3	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990SD-1.2/NOPB	WSO	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP3990SD-1.5/NOPB	WSO	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP3990SD-1.8/NOPB	WSO	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP3990TL-0.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-1.2/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-1.35/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-1.5/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3990TL-1.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-2.5/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-2.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-0.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-1.2/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-1.35/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-1.5/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-1.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-2.5/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-2.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



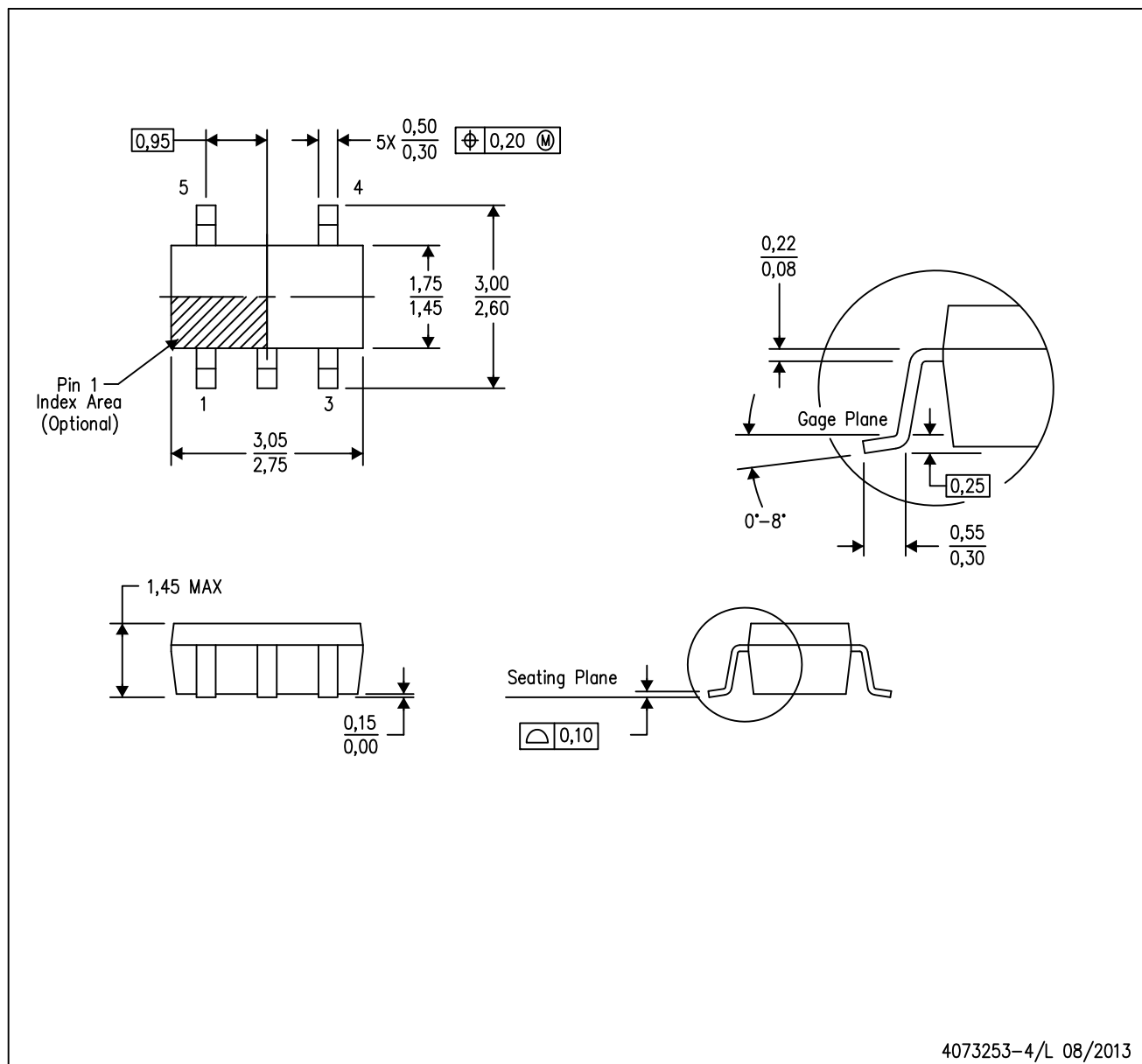
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3990MF-1.2/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3990MF-1.8	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3990MF-1.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3990MF-2.5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3990MF-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3990MF-2.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3990MF-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3990MFX-1.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3990MFX-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3990MFX-3.3	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3990MFX-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3990SD-1.2/NOPB	WSO	NGG	6	1000	210.0	185.0	35.0
LP3990SD-1.5/NOPB	WSO	NGG	6	1000	210.0	185.0	35.0
LP3990SD-1.8/NOPB	WSO	NGG	6	1000	210.0	185.0	35.0
LP3990TL-0.8/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3990TL-1.2/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3990TL-1.35/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3990TL-1.5/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3990TL-1.8/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3990TL-2.5/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3990TL-2.8/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3990TLX-0.8/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3990TLX-1.2/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3990TLX-1.35/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3990TLX-1.5/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3990TLX-1.8/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3990TLX-2.5/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3990TLX-2.8/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0

DBV (R-PDSO-G5)

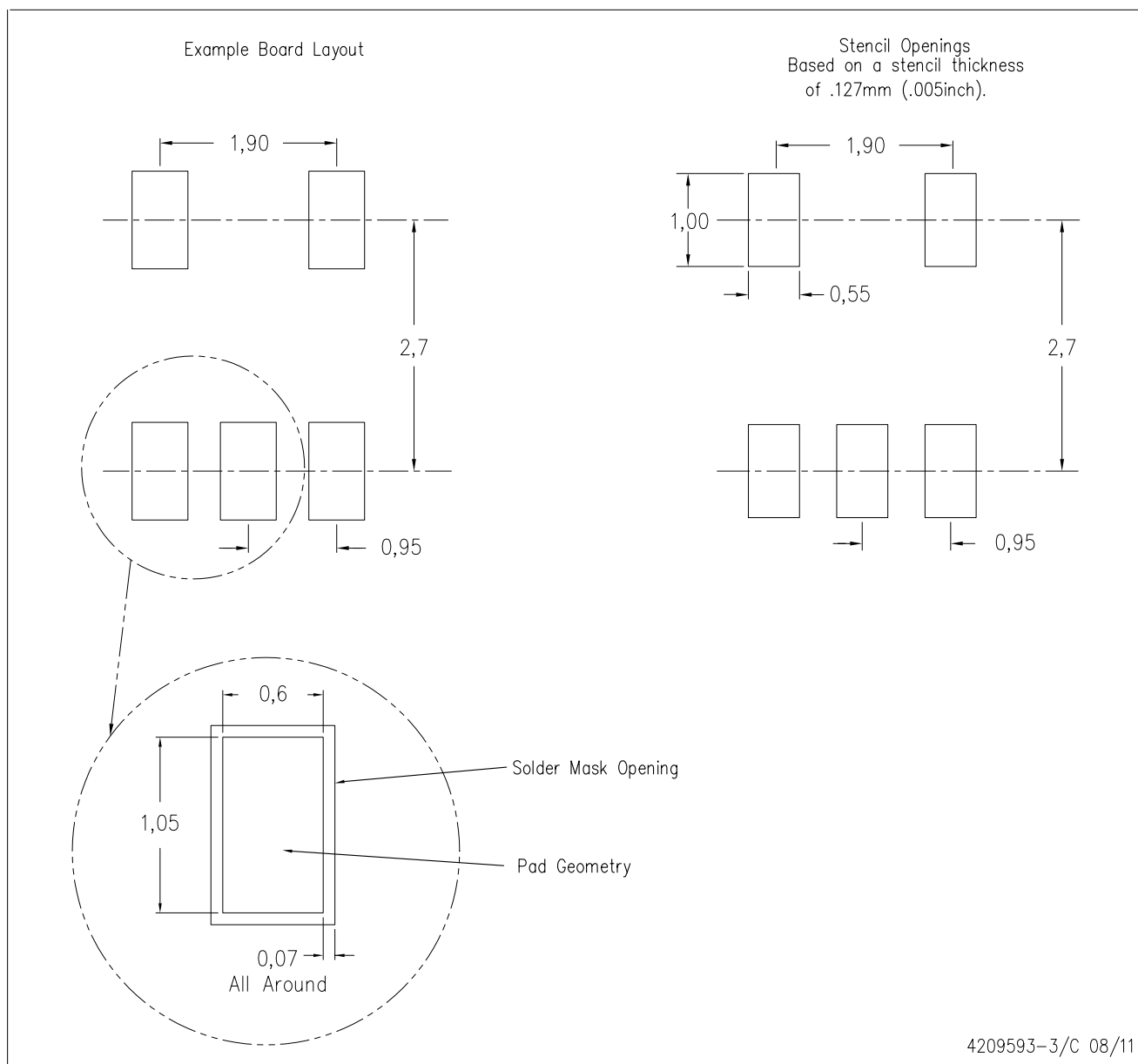
PLASTIC SMALL-OUTLINE PACKAGE



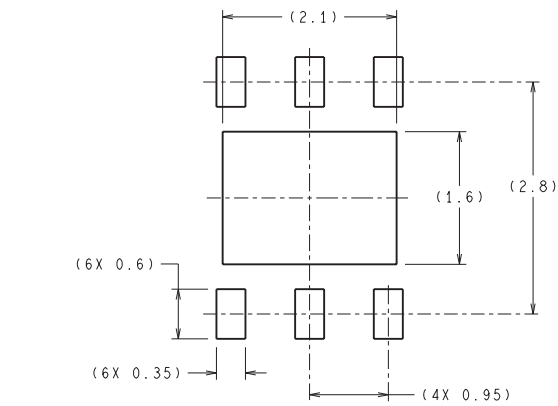
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

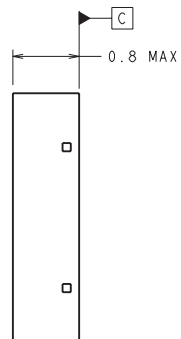
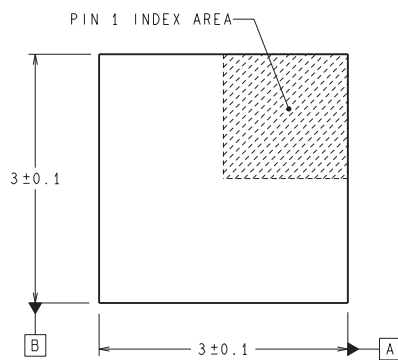
PLASTIC SMALL OUTLINE



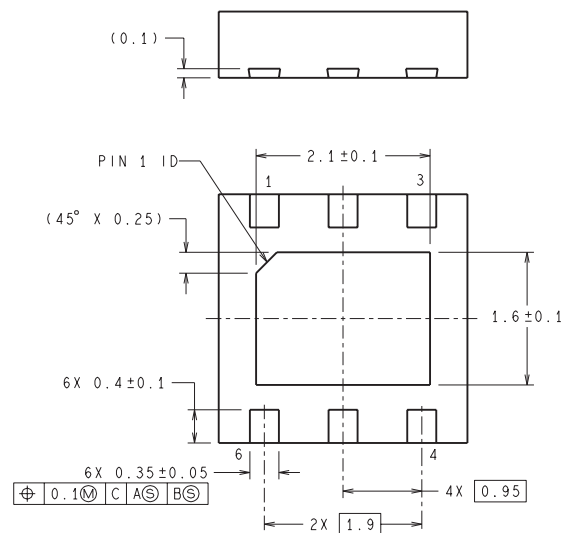
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



RECOMMENDED LAND PATTERN

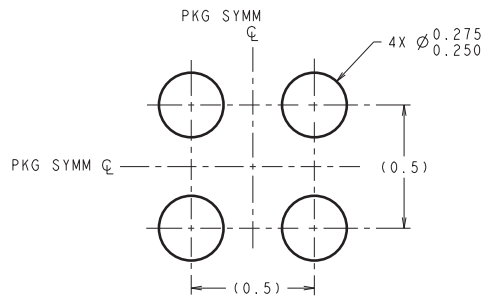


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DIMENSION IN () FOR REFERENCE ONLY



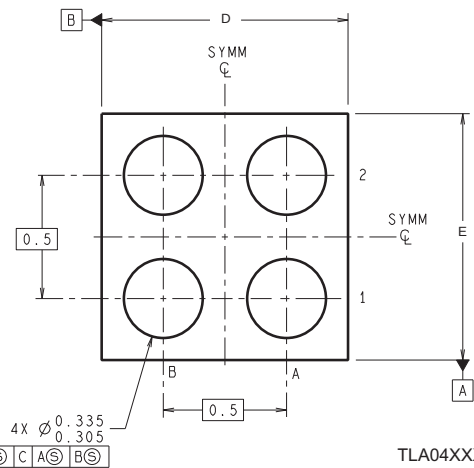
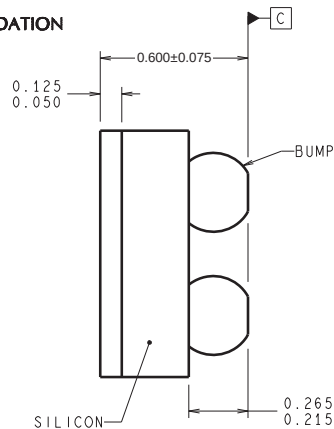
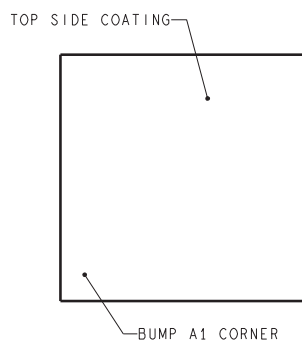
SDE06A (Rev A)

YZR0004



DIMENSIONS ARE IN MILLIMETERS
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LAND PATTERN RECOMMENDATION



TLA04XXX (Rev D)

D: Max = 1.324 mm, Min = 1.263 mm

E: Max = 1.045 mm, Min = 0.984 mm

4215042/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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